High-Speed Millimeter-Wave Modulator/Demodulator

by

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ABSTRACT

We report for the first time on the performance of a millimeter-wave quaternary phase shift keyed (QPSK) modulator/demodulator at information rates up to 8 Gbit/s. The circuits operate in the 40 GHz range and are subharmonically pumped by local oscillators at half the carrier frequencies. The demodulated output data streams showed clean eye diagrams with corresponding bit error rates of less than 10^{-11} up to the highest rate measured (8 Gbit/s total information rate).

I. INTRODUCTION

Quaternary phase modulators have been described in the literature [1-3]. The most popular high data-rate modulators employ switching lengths of transmission lines to obtain desired phase shifts. A modulator of this type has been reported by Glance and Amitay [4] with low insertion loss at 12 GHz and data rates up to 0.8 Gbit/s. Path length modulators cannot be used as demodulators, however, and little attention has been given to demodulators for QPSK modulated signals. In a recent paper we reported on a different kind of high-speed QPSK modulator which can also operate as a demodulator [5] at a carrier frequency of 13 GHz. A tandem circuit pair enabled modulation and recovery of data up to 3.6 Gbit/s with bit error rates less than 10^{-11}. The modulator/demodulator was initially constructed for operation at 13 GHz to enable circuit components to be characterized with a network analyzer having a maximum frequency of 18 GHz prior to integrating the components on a single substrate. After characterization of the units at 13 GHz, the circuit has now been scaled for operation at 40 GHz by reducing all dimensions by a factor of 3 with only minor modifications. This work demonstrates the applicability of scaling of hybrid circuits into the millimeter-wave frequency range.

A schematic diagram of the modulator is shown in Fig. 1. The circuit consists basically of a local oscillator at half of the carrier frequency, two identical mixers and a summing network. Two incoming non-return to zero bit streams arrive at rates up to 4 Gbit/s or higher to their respective mixers where they generate local oscillator second harmonics at phases dependent upon the state of the bit. Each mixer consists of a nonlinear device with a current-voltage characteristic having a center of symmetry, i.e., $i(v) = -i(-v)$, where i is the instantaneous current through the mixer and v the voltage across the mixer. This characteristic can be achieved with two Schottky diodes in an antiparallel connection [5]. Both mixers are fed from the same local oscillator at 19 GHz but with a phase difference of $\pi/4$ to achieve proper phase relation of the upconverted bit streams, which, after summation in the Σ network, result in a QPSK signal with a center frequency close to 40 GHz.

II. THEORY OF OPERATION

The mixing and upconversion of the two non-return-to-zero (NRZ) bit streams in the circuit of Fig. 1 result in a QPSK signal out of the summing port at twice the local oscillator frequency. We assume that the two identical mixers are resistive with a nonlinear current-voltage characteristics given by

$$i = \sum_{k=0}^{\infty} a_{2k+1} v^{2k+1} , \tag{1}$$

which satisfies the requirement that $i(v) = -i(-v)$. Other than the first term in the series which is linear and does not result in frequency conversion, all other terms will produce mixing products at twice the local oscillator frequency. As an illustration we shall consider only the term for $k=1$ for which $i = a_3 v^3$. If the local oscillator frequency is f, the voltages across the lower (M_I) and upper (M_Q) mixers in Fig. 1 are

$$v_I = \sin(2\pi ft) + \delta v_I(t) , \tag{2}$$

$$v_Q = \sin(2\pi ft - \pi/4) + \delta v_Q(t) , \tag{3}$$

where $\delta v_I(t)$ and $\delta v_Q(t)$ are the pulse sequences containing the modulation information. These separate pulse trains are fed to the inputs labeled I and Q shown in Fig. 1 (in phase rail and quadruture phase rail). The current flowing in the lower mixer is then

$$i_I = v_I^3 = (sin2\pi ft + \delta v_I)^3 , \tag{4}$$

where the proportionality constant a_3 has been ignored giving

$$i_I = \sin^3 2\pi ft + 3\delta v_I \sin^2 2\pi ft + \cdots . \tag{5}$$

The second term in this expansion contains the second harmonic modulation information which can be expressed as $3\delta v_I(1-\cos 4\pi ft)/2$. The second harmonic component is

$$i_I = -3\delta v_I \cos(4\pi ft)/2\ , \tag{6}$$

which is the product of the bit voltage and the second harmonic of the local oscillator.

Similarly the corresponding current component in the upper rail is

$$i_Q = -3\delta v_Q \sin(4\pi ft)/2\ . \tag{7}$$

The current emerging from the summing network $\sum$ is

$$i = 3\{-\delta v_Q \sin(4\pi ft) - \delta v_I \cos(4\pi ft)\}\ . \tag{8}$$

Since each bit stream can have two states

$$\delta v_I = \pm d \text{ and } \delta v_Q = \pm d \tag{9}$$

we obtain four possible phase states in quadrature corresponding to QPSK modulation.

The circuit of Fig. 1 will also demodulate a QPSK modulated signal. If the modulated signal enters the summing port, the two NRZ bit streams corresponding to the bit streams impressed on each rail of the modulator will be recovered without crosstalk on the data rails provided that the local oscillator is properly phased with respect to the QPSK signal.

Consider a QPSK modulated signal voltage given by

$$v = -\delta v_Q \sin(4\pi ft) - \delta v_I \cos(4\pi ft) \tag{10}$$

impressed upon each of the two mixers. The local oscillator voltage on the lower mixer is proportional to $\sin(2\pi ft)$, and the voltage on the mixer is the sum of the modulated signal and local oscillator voltage. The current out of the lower mixer is

$$\begin{aligned} i &= v^3 \\ &= \{\delta v_Q \sin(4\pi ft) - \delta v_I \cos(4\pi ft) + \sin(2\pi ft)\}^3 \end{aligned} \tag{11}$$

Terms in the expansion of (11) which do not depend upon f are the bit stream components recovered on the lower rail. The only component not involving f arises from the term $-3\delta v_I \cos(4\pi ft)\sin^2(2\pi ft)$ which further reduces to $3\delta v_I/4$. On the upper mixer the voltage applied is

$$i = \{-\delta v_Q \sin(4\pi ft) - \delta v_I \cos(4\pi ft) + \sin(2\pi ft - \pi/4)\}^3\ . \tag{12}$$

The data stream term is $-3\delta v_Q \sin(4\pi ft)\sin^2(2\pi ft - \pi/4)$ which reduces to $3\delta v_Q/4$. Since the current on the lower rail involves only δv_I and that on the upper rail is a function of δv_Q only, the two data streams can be recovered without crosstalk. The phase of the local oscillator was selected for recovery of the data on the rails corresponding to those in the modulator. For some other discrete phases the bit streams can be recovered without crosstalk but inverted in phase or on opposite rails, however there is intersymbol interference on the recovered data trains for other arbitrary phases.

III. CIRCUIT CONSTRUCTION

The circuit pattern was reduced in size by a factor of three from the 13 GHz circuit. A modulator unit for 38 GHz is shown in Fig. 2. Before reduction, modifications were made to the 13 GHz mask patterns to accommodate the mixer diodes and to allow the data ports to enter the housing from the sides so as not to interfere with the waveguide flange at the local oscillator input port. The substrate was 0.010 in. thick RT/Duroid 5880, and the housing was reduced in size by a factor of three from the 13 GHz unit and altered to suit the substrate changes.

Both silicon and gallium arsenide Schottky barrier diodes were used as mixers in both modulator and demodulator units. Silicon devices, Hewlett-Packard types HP5510 (medium barrier height) and HP5530 (low barrier height) are available in a dual diode tee configuration which allows antiparallel connection by joining the arms of the tee together. Gallium arsenide Alpha type DMK3307 is a two terminal antiparallel connected diode pair, and Marconi type DC1346M is a single diode with two units antiparalleled for a symmetrical mixer characteristic.

IV. PERFORMANCE

The output of modulator-demodulator tandem pairs was maximized by varying both local oscillator power to each unit and data stream drive to the modulator. Data trains out of the pair are shown in Fig. 3 at a 50 Mbit/s data rate. Intersymbol distortion has been minimized by adjusting the phase difference of the local oscillator between the I and the Q mixers for both modulator and demodulator with dielectric loading on one of the local oscillator fin lines. It was necessary to trim the phase individually for each set of mixers and to a smaller degree for the drive levels of both bit stream and local oscillator on all units. Some crosstalk is evidenced by small sharp pulses on each rail during a switch in states on the other rail. This results from reactive parasitics in the modulating diodes. This kind of crosstalk was more pronounced for silicon mixers than for gallium arsenide units. Measurements above 2 Gbit/s necessitated the use of a time division multiplexer described by Gnauck [6]. Eye diagrams at 3 and 4 Gbit/s on each rail are shown in Figs. 4 and 5 and are quite open. Bit error rates were less than 10^{-11} up to 4 Gbit/s per rail which was the highest data rate tested.

Silicon mixers had slightly lower overall conversion loss for the modulator-demodulator pair, but gave lower output bit stream signals than gallium arsenide mixers. The best conversion losses with the largest output were obtained for silicon units with HP5530 (low barrier) diodes in the modulator and HP5510 (medium barrier) devices in the demodulator. Best results were obtained for gallium arsenide units with DMK3307's in the modulator and DC1346M's in the demodulator. Both silicon modulator and demodulator units required more local oscillator power than the corresponding gallium arsenide devices. A comparison of operating conditions for units with silicon and gallium arsenide mixers is given in Table 1.

V. CONCLUSIONS

A new millimeter-wave modulator operating at carrier frequencies in the 40 GHz frequency range has been devised, designed and tested. We have experimentally confirmed

operation with low error rates up to 4 Gbit/s per rail which gives an information rate of 8 Gbit/s. The performance of modulator-demodulator pairs is given in the table with a comparison of operating conditions for units with both Si and GaAs subharmonically pumped mixers.

VI. ACKNOWLEDGMENT

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Table 1 CIRCUIT PERFORMANCE

OPERATING CONDITIONS

	GaAs diodes	Si diodes
Bit Stream Input Levels	±320 mV	±160 mV
Bit Stream Output Levels	±7.5 mV	±4.5 mV
Modulator Output Power	−11 dBm	−14 dBm
Conversion Loss		
Modulator	17 dB	14 dB
Demodulator	14 dB	15 dB
Carrier Frequency	38 GHz	38 GHz
Local Oscillator		
Frequency	19 GHz	19 GHz
Power - Modulator	13 dBm	14 dBm
- Demodulator	10 dBm	12.5 dBm

TEST RESULTS

Bit Rate/Rail (maximum tested)	4 Gbit/s
Total Information Rate (maximum tested)	8 Gbit/s
Error Rate (50 Mbit/s - 4 Gbit/s per rail)	$< 10^{-11}$

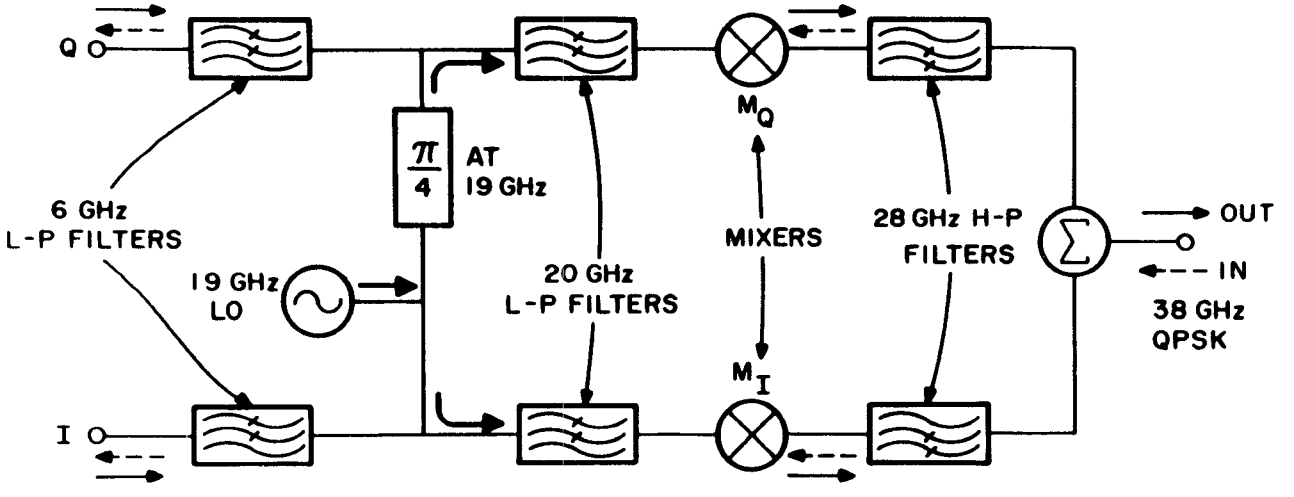

Fig. 1 Detailed schematic of the 38 GHz modulator/demodulator showing filters for routing signals. Solid arrows show direction of signal flow in the modulator and dotted arrows in the demodulator. The 6 GHz low-pass filters pass the baseband data streams but reject the local oscillator. The local oscillator coupling to the Q and I rails is inherently a high-pass network which rejects the data stream from the local oscillator feed lines. The 20 GHz low-pass filters pass the data streams and local oscillator but reject mixer products. The 28 GHz high-pass filters reject data streams and local oscillator but pass the 38 GHz QPSK modulated signal.

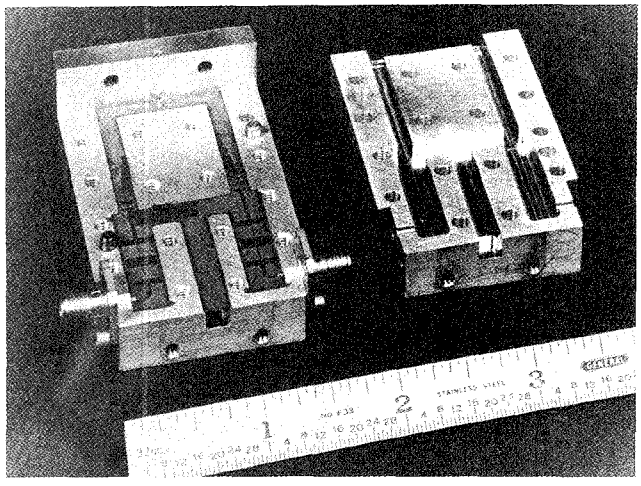

Fig. 2 38 GHz modulator/demodulator with the top of the housing removed. Channels in the housing provide shields for the microstrip elements. They are also part of the finline structure and of the waveguide in the 28 GHz high-pass filters. Unlike the 13 GHz structure, the data ports had to be brought out of the sides of the housing rather than the end to avoid interference with the waveguide flange from the local oscillator feed. The small amount of dielectric loading added to one of the local oscillator fin lines appears on the substrate on the left-hand side of the branch.

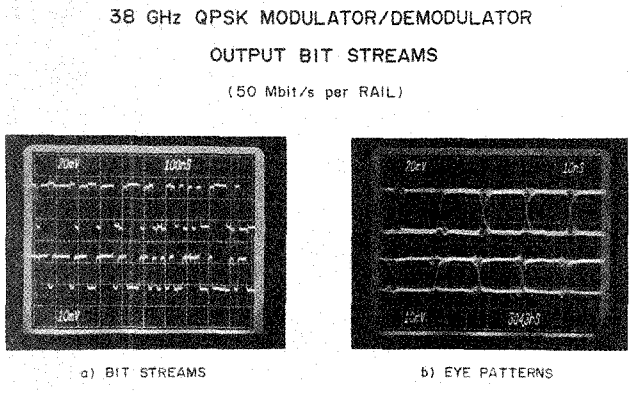

Fig. 3 Output pulse trains and eye diagrams of a modulator-demodulator circuit pair measured at in-phase and quadrature (I and Q) ports of the demodulator. The pulses are generated with 50 Mbit/s pseudo-random input data streams from an HP7780A pulse pattern generator. Some crosstalk is evident by sharp pulses in each data train when the state of the other train changes. The crosstalk is caused by non-idealities in the beam-leaded Schottky barrier switching diodes. This results in a displacement of the data points from their reference points in the signal space of the carrier. The eye diagrams obtained from both output rails of the demodulator are open, and the transitions are well defined with bit error rates lower than 10^{-11}.

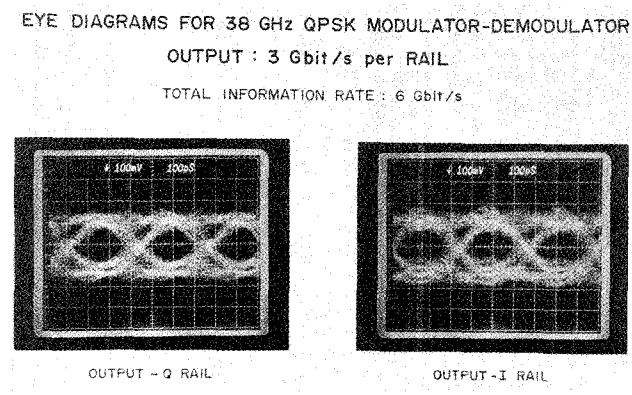

Fig. 4 Output pulse waveforms (eye diagrams) for a 38 GHz modulator-demodulator circuit pair at data rates of 3 Gbit/s on each rail. The total information rate of the circuit is 6 Gbit/s and the diagrams are sufficiently clean to achieve a bit error rate of 10^{-11}. The pulses are generated with an Anritsu MG642A pulse pattern generator, and the bit error rate was measured with the MS65A error detection set. The output from the Anritsu pattern generator is limited to a rate of 2 Gbit/s and was doubled by means of an in-house high-speed logic circuit. In order to achieve coherent detection, a line stretcher was used to provide the correct local oscillator phase to drive the demodulator circuit.

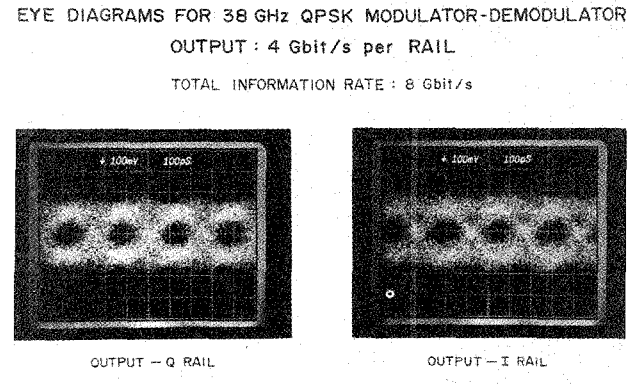

Fig. 5 Output pulse waveforms for 38 GHz modulator-demodulator circuit pair at data rates of 4 Gbit/s on each rail. The diagrams remain sufficiently clean to achieve bit error rates of 10^{-11} for a total information rate of 8 Gbit/s. The tests were performed with an Anritsu MG642A pulse pattern generator followed by a high-speed in-house doubler. The doubled pulse stream was split into two separate streams which were subsequently interleaved after delaying one stream by an appropriate multiple of the clock rate. The figure shows that the degradation of the eye patterns is not significantly worse compared with those at a data rate of 3 Gbit/s. The performance of the circuit is limited by the speed and parasitics of the switching diodes in the modulator/demodulator circuits and the cutoff frequency of the low-pass filter.